A GaAs HBT MONOLITHIC LOGARITHMIC IF (0.5 TO 1.5 GHz) AMPLIFIER WITH 60 dB DYNAMIC RANGE AND 400 mW POWER CONSUMPTION

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ABSTRACT

A GaAs/AlGaAs HBT monolithic successive-detection logarithmic IF amplifier (SDLA) is described which demonstrates significant reduction in size and power consumption over state-of-the-art Si bipolar and GaAs MESFET log amps with comparable dynamic range and IF bandwidth. This work was motivated by electronic warfare channelized receiver applications in which size, power, and cost are key drivers. The GaAs HBT SDLA log amp achieves single-chip (1.2x2.4 mm^2) dynamic range >60 dB (-55 to +5 dBm) with $\leq \pm 1$ dB error over 1 GHz IF bandwidth at temperatures up to 125 °C while consuming less than 400 mW of power.

INTRODUCTION

In certain electronic warfare (EW) channelized receiver applications, log amplifiers are required which have high performance combined with miniaturization and ultra-low power consumption. Present state-of-the-art log amplifiers based on Si bipolar technology are complex hybrid circuits. The GaAs HBT's intrinsically larger gain-bandwidth and semi-insulating substrate facilitates higher IF frequency implementation which results in the ability to detect narrower pulses. It also permits more compact analog components such as filters and integrable coupling capacitors. The HBT's intrinsic small delay-power product allows speed to be traded off for lower power operation at IF frequencies. The small-scale integration requirement of the SDLA is consistent with high yield, producibility, and low cost for the GaAs HBT technology.

Logarithmic IF amplifiers based on the successive-detection architecture are usually employed when wide instantaneous dynamic range (>60 dB) and good fidelity for pulsed RF signals (less than 50 ns rise time) are required. Bipolar transistors offer attractive advantages over field-effect transistors for such log amp applications. These include exponential-based nonlinear function, better device matching, higher transconductance and output impedance for higher gain and lower distortion, and lower trapping effects and 1/f noise. Silicon bipolar technology has dominated the log amplifier application area with these intrinsic advantages facilitating relatively easy implementation of two key receiver functions, limited IF phase detection and detected logarithmic compression, into the same component assembly. However, the highest performance silicon bipolar designs are currently limited to 800 MHz bandwidth, >2 W power consumption, and hybrid complexity [1].

The GaAs HBT offers improved speed, power, and gain performance with significantly relaxed fabrication requirements. Relaxed emitter lithographic dimensions of about 3 μm are adequate to achieve HBT transistors with f_T and f_{max} in the range of 15-30 GHz. GaAs HBT technology has already demonstrated improved performance [2] over advanced GaAs MESFET implementations [3] for true logarithmic amplifiers, which output the logged, undetected IF input signal; this work extends GaAs HBT state-of-the-art performance to successive detection-type logarithmic amplifiers as well. For the same dynamic range, GaAs HBT offers monolithic SDLA with significantly improved bandwidth, power consumption, and size over Si bipolar SDLAs.

MONOLITHIC SDLA DESIGN

The successive-detection logarithmic function [4] is achieved in a piecewise-linear approximation using series linear amplifiers and parallel logging detectors (Fig. 1). The piecewise-linear combination of the logging detectors reduces the log linearity required for each individual detector. The AC coupling capacitors between linear amplifier stages are needed in the the successive-detection architecture to prevent the offset voltage of the first linear amplifier from saturating the last detector. Integration of these coupling capacitors at 50-100 MHz, typically the low end of silicon-based SDLA bandwidths [1], consumes too much die area. The low end of the GaAs HBT SDLA operating bandwidth, 500 MHz, is more than half the operating bandwidth of comparable silicon hybrid amplifiers.

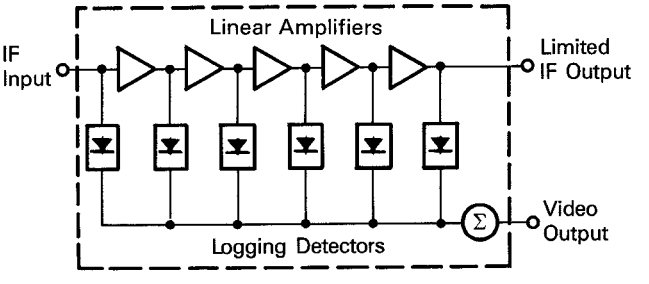

Fig. 1. GaAs HBT successive detection logarithmic amplifier (SDLA) block diagram.

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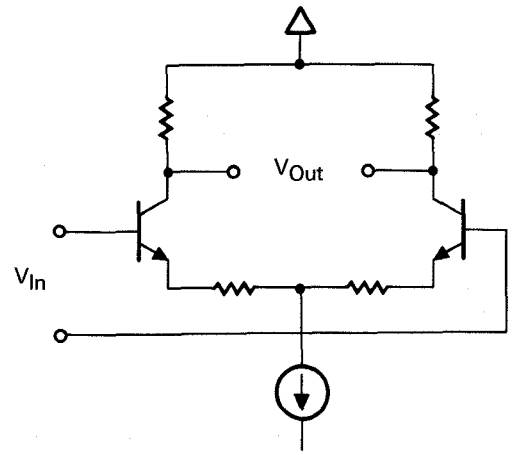

Fig. 2. Differential pair used as SDLA building block linear amplifier.

The five series linear amplifiers, shown in Fig. 1, are implemented as simple differential pair amplifiers (Fig. 2), and produce approximately 60 dB of small-signal gain. A constant phase, constant amplitude, limited IF output needed for some applications is also available. Logarithmic rectification (detection) of the IF signal is performed at high frequency by a full-wave detector circuit. The transconductance of the SDLA detector is approximately logarithmic even at high frequencies (>2 GHz), providing for detector transient response with fast rise and fall times. Addition of the detector in parallel with the first linear amplifier stage extends the top of the dynamic range to about +5 dBm. The detected current I_{OUT} from the logging detectors is filtered by a single-pole RC low-pass filter, which determines the output video bandwidth. An output emitter follower following the RC filter completes the video buffer.

GaAs HBT SDLA FABRICATION

The monolithic SDLAs were fabricated with a 3-μm emitter, self-aligned base ohmic metal (SABM) HBT IC fabrication process designed for baseband/RF analog applications, previously reported in detail [2]. The mesa HBT IC process incorporates Npn transistors, nichrome thin-film resistors, and metal-insulator-metal capacitors which are isolated using boron damage implantation and integrated using a double-level interconnect metal. Molecular-beam epitaxy is used for the HBT device structure. This process has already demonstrated state-of-the-art microwave amplifiers and oscillators [4]. DC current gain ß≈50 and high f_T and f_{max} (15-30 GHz) at low collector current density J_C≈3 kA/cm^2 (Fig. 3) combine to provide high accuracy RF/analog and high speed digital performance. The SPICE transistor model for the standard HBT, with a 3x10-μm^2 emitter, is shown in Fig. 4.

The fabricated GaAs HBT SDLA shown in Fig. 5 contains 129 HBTs and occupies a die size of 1.2x2.4 mm^2.

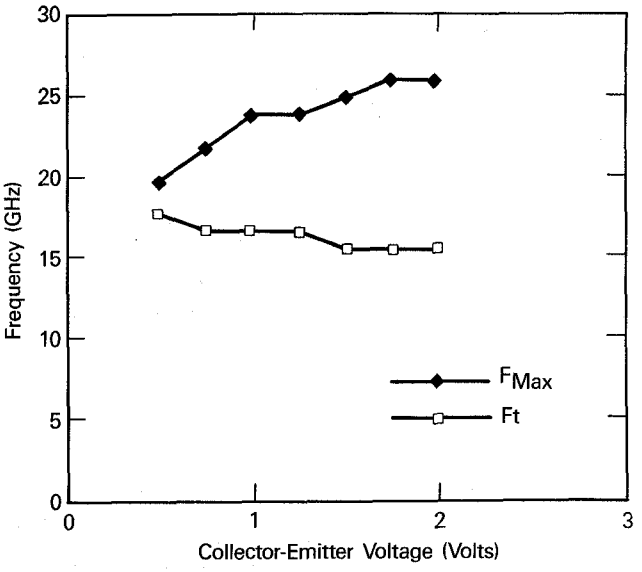

Fig. 3. f_T and f_{max} vs. V_{CE} for 3x10μm^2-emitter HBT at I_C=1 mA.

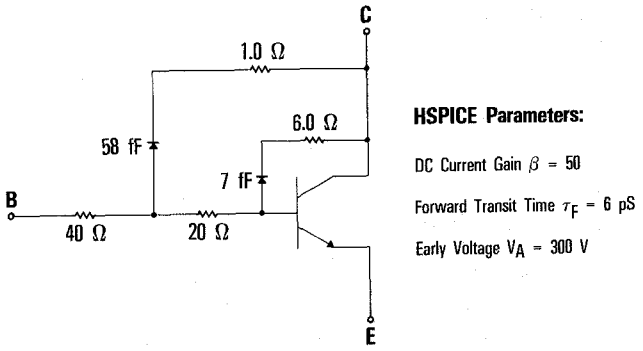

Fig. 4. SPICE model for self-aligned base ohmic metal HBT with 3x10μm^2-emitter.

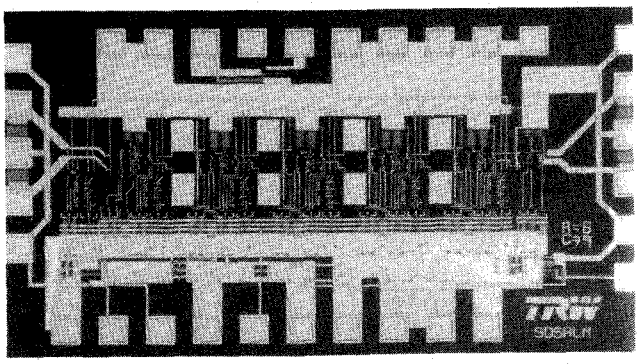

Fig. 5. Photomicrograph of monolithic GaAs HBT SDLA (129 transistors; chip size: 2 mm x 1mm).

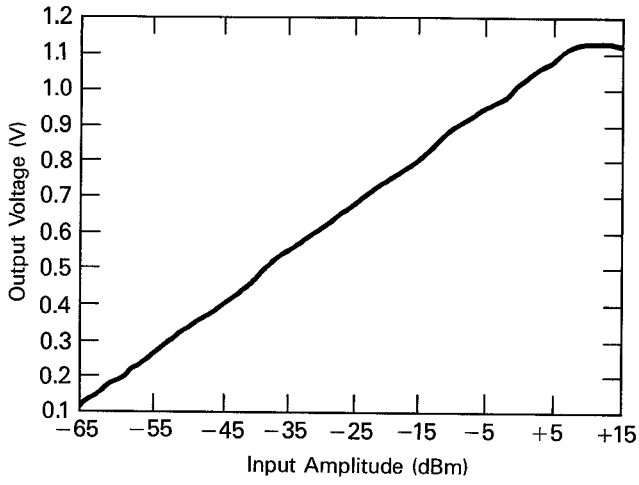

Fig. 6. Log transfer function for IF input frequency of 750 MHz.

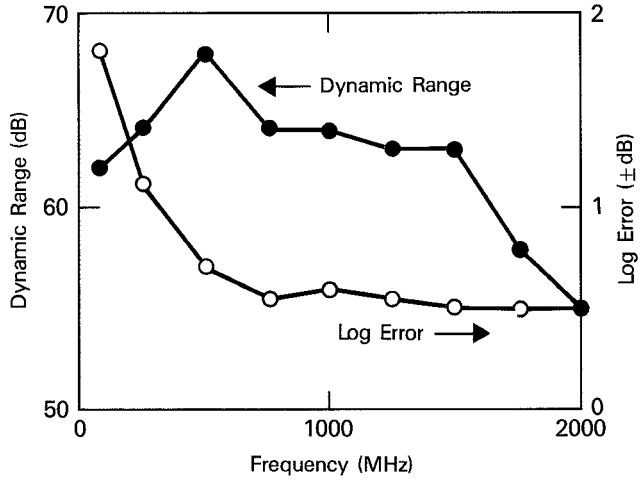

Fig. 7. GaAs HBT SDLA linearity and dynamic range vs. frequency.

MONOLITHIC SDLA PERFORMANCE

Log transfer functions (Fig. 6) for IF input frequencies from 100 MHz to 2 GHz were measured with the amplifier driving a low-pass filtered high impedance load (digital voltmeter). All circuit testing was performed on-wafer using a ceramic blade microstrip probe card. Total amplifier power was 365 milliwatts from ±5 volt supplies. Dynamic range greater than 60 dB with integral nonlinearity less than ±1 dB was obtained over more than 1 GHz of bandwidth (Fig. 7). Proportional-to-temperature current source biasing for the linear amplifier stages, needed to maintain constant gain over temperature, was not included in the present iteration. When the current in the linear differential pair amplifiers was externally varied proportionally to temperature, the log error at the elevated temperature of 125°C degraded slightly over the room temperature response as shown in Fig. 8.

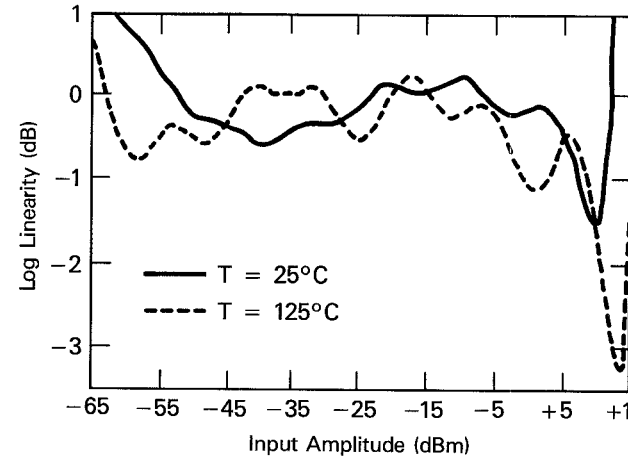

Fig. 8. Comparison of log error for 750 MHz IF input frequency at 25°C and 125°C.

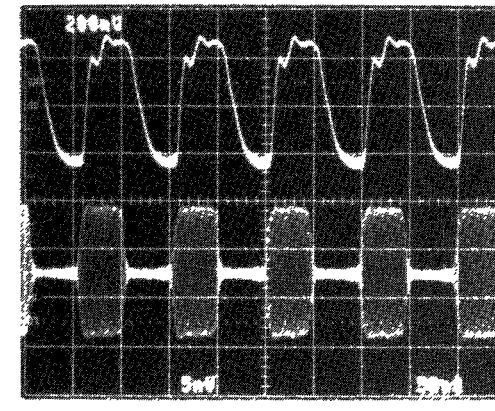

Fig. 9. SDLA response (Top, V:200 mV/div) for -20 dBm, 750 MHz IF pulse 50 ns wide (Bottom, 5 mV/div) at 10 MHz repetition rate (H: 50 ns/div).

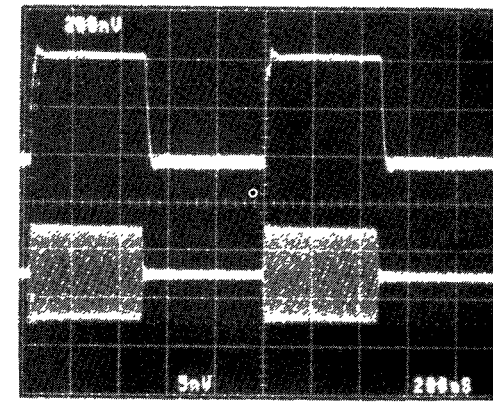

Fig. 10. SDLA response (Top, 200 mV/div) for -20 dBm, 750 MHz IF pulse 500 ns wide (Bottom, 5mV/div) at 1 MHz repetition rate (H: 200 ns/div).

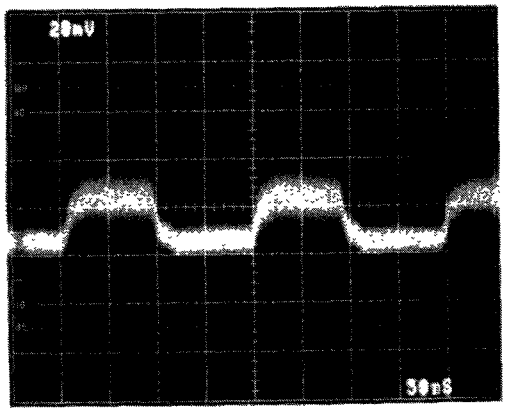

Fig. 11. Tangential signal sensitivity (TSS) for -66 dBm, 750 MHz IF pulse 100 nsec wide at 5 MHz repetition rate (V: 20mV/div, H: 50 ns/div).

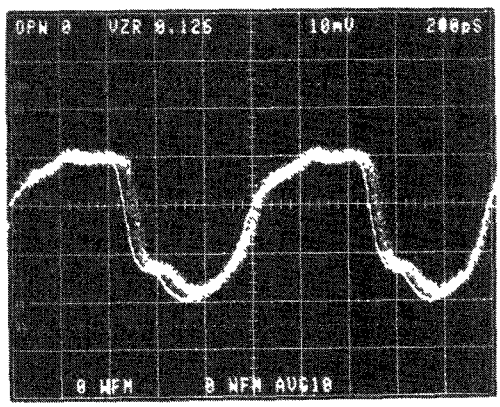

Fig. 12. Limited IF output phase variation for +5 dBm (sharp trace) and +55 dBm (blurred trace) inputs at 1 GHz input (V: 10mV/div, H: 50 ns/div).

The monolithic log amp can accurately process pulsed RF carriers 50 ns wide spaced 50 ns apart (Fig. 9). 10-90% risetime at the video output driving a heavily capacitive high impedance input to an oscilloscope with 200 MHz bandwidth was less than 20 ns and the 10-90% fall was less than 40 ns. The ringing in Fig. 9 is caused by the emitter follower video buffer driving the heavy capacitive load. Figure 10 shows the amplifier response to a 750 MHz, -20 dBm pulse 500 ns wide. Tangential signal sensitivity (TSS) was -66 dBm (Fig. 11). The phase response of the IF output varied less than 22 degrees over 60 dBm of input dynamic range at 1 GHz IF input frequency (Fig. 12).

The monolithic GaAs SDLA performance is summarized in Table 1.

SUMMARY AND CONCLUSIONS

A GaAs/AlGaAs HBT monolithic successive-detection logarithmic IF amplifier (SDLA) have been demonstrated which offers significant reduction in size and power consumption over state-of-the-art Si bipolar and GaAs MESFET log amps with comparable dynamic range and IF bandwidth. This work was motivated by electronic warfare channelized receiver applications in which size, power, and cost are key drivers. The GaAs HBT SDLA log amp achieves single-chip (1.2x2.4 mm^2) dynamic range >60 dB (-55 to +5 dBm) with $\leq \pm 1$ dB error over 1 GHz IF bandwidth at temperatures up to 125 °C while consuming less than 400 mW of power.

Table 1
GaAs HBT SDLA Performance Summary

Dynamic Range	-55 dBm to +5 dBm
If Input Frequency	0.5 to 1.5 GHz
Power	400 mW
Log Error	$< \pm 1$ dB
Tangential Signal Sensitivity (TSS)	-66 dBm
Video Bandwidth	20 MHz
Video Risetime (10 to 90%)	<20 nsec
Video Fall Time (10 to 90%)	<40 nsec
Phase Variation Over -55 to +5 dBm, 1 GHz IF	22°
Power Supplies	± 5 Volts
Integration Level	Monolithic

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REFERENCES

[1] J. Browne, "Wide-Ranging Hybrid Logamps Rise Quickly," *Microwaves & RF*, vol. 27, pp. 207-213, 1988.

[2] A. K. Oki, M. E. Kim, G. M. Gorman, and J. B. Camou, "High-performance GaAs heterojunction bipolar transistor monolithic logarithmic IF amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, pp. 1958-1965, Dec. 1988.

[3] M. A. Smith, "A GaAs Monolithic True Logarithmic Amplifier for 0.5 to 4 GHz Applications," *Microwave and Millimeter-Wave Monolithic Circuits Symposium Tech. Dig.*, pp. 37-40, 1988.

[4] R. S. Hughes, *Logarithmic Amplification With Application to Radar and EW*, Artech House, Inc., Dedham, 1986.

[5] M. E. Kim, A. K. Oki, J. B. Camou, P. D. Chow, B. L. Nelson, D. M. Smith, J. C. Canyon, C. C. Yang, R. Dixit, and B. R. Allen, "12-40 GHz low harmonic distortion and phase noise performance of GaAs heterojunction bipolar transistors," in *1988 IEEE GaAs IC Symp. Dig.* (Nashville), Nov. 1988, pp. 117-120.